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ADVANCED MICRODISPLAYS FOR PORTABLE SYSTEMS

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August 1999

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This report documents the development of extremely integrated miniature display technology and high performance electronics alongside active-matrix circuitry. The goal of this development was to produce an absolutely portable platform to support imaging and video messaging for use with head-mounted and hand-held systems. Extreme complementary metal oxide semiconductor (CMOS) integration, using new low-power CMOS technology, in the enabling technology behind the display systems developed under this program. This program has demonstrated the capability of extreme display system integration by incorporating active matrix pixel arrays, interface logic (asynchronous serial, RS-170), font memory, programmable microprocessors, NTSC, JPEG, and MPEG application specific integrated circuits (ASIC) decoders, and lamp, electro-luminescent (EL), and light emitting diode (LED) illumination drive circuitry into a single display backplane.

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PREFACE

This report describes the development of extremely integrated miniature display technology that uses high performance application specific digital and analog electronics alongside active-matrix display circuitry and drive electronics. The goal of this development was to produce an absolutely portable platform to support imaging and video messaging for use with head-mounted and hand-held systems, wherein the enabling technology is the integrated MicroDisplay device. A portion of this development effort included a subcontract with the Information Sciences Institute (ISI), a University of Southern California research facility, for the development and fabrication of a programmable microcontroller that could be integrated with a MicroDisplay device. Contract support was provided by the U.S. Army Soldier Systems Command (USASSCOM) and the Defense Advanced Research Projects Agency (DARPA), contract DAAK60-96-C-3025. Project work was conducted between June 1996 and May 1998 (with a no-cost extension through October 1998).

The MicroDisplay Corporation would like to thank DARPA Agent Mr. Henry Girolamo of USASSCOM and DARPA Program Manager Mr. Ellison Urban of DARPA/ETO for their outstanding guidance in the management of this project.

SUMMARY

The primary focus of this project has been to make possible the creation of personal computing and communication devices with embedded miniature information displays and optical systems in a highly reduced packaging form-factor. Based on technology developed at The Massachusetts Institute of Technology (MIT), the complete display systems maximize performance, durability, integration, and manufacturability while minimizing power dissipation, size, packaging, and cost.

Historically, display systems have been the limiting factor for portable computing and communication products. Current flat panel display technology comes tied to cumbersome, power and space-hungry driver boards. Smart, compact and power-efficient display systems make possible head-mounted and body-worn communication and computing tools.

Extreme complementary metal oxide semiconductor (CMOS) integration, using new low-power CMOS technology, enables our sophisticated display systems. This program has successfully demonstrated the capability of extreme display system integration by incorporating active matrix pixel arrays, interface logic (asynchronous serial, RS-170), font memory, programmable microprocessors, NTSC, JPEG, and MPEG application specific integrated circuits (ASIC) decoders, and lamp, electro-luminescent (EL), and light emitting diode (LED) illumination drive circuitry into a single display backplane.

Deliverables for this project were as follows:
Year 1 - Micro Video Integrated MicroDisplay
Year 2 - Universal MicroDisplay Integrated Display and Microcontroller Technology

ADVANCED MICRODISPLAYS FOR PORTABLE SYSTEMS
1 INTRODUCTION

Project Objectives

The objective of this contract has been the iterative miniaturization of electronic displays and component developments that can be integrated into head-mounted and hand-held products to display sensory and tactical data to soldiers in combat or peacekeeping missions. The development of integrated microdisplays is expected to make possible the creation of personal computing and communicating devices with embedded displays, in optical systems in a highly miniaturized form.

Project Approach

The proposed micron-scale Advanced MicroDisplay technology was designed to immediately replace current LCD displays in ultra-portable systems, with little change in form-factor, other than a general reduction in size and power consumption. Replacing current high-resolution LCD's and their associated electronics with a single standard-process CMOS chip would have direct savings in power, mass, and reliability. The fabrication cost of a single-chip device is currently around five dollars per chip in quantity, and is expected to drop as technology advances. This low production cost could make personal information devices almost disposable.

The current state of silicon-compiler technology has allowed the development of an automated display compiler system and an optical distortion compiler system that, together, can place and scale pixel arrays to compensate for arbitrary optical distortion functions. This could possibly be extended to fresnel or lenslet-type optical systems of even lighter weight and greater functionality. This precision automated layout control has also enabled smaller device packages with fewer lenses of shorter focal lengths.

As VLSI fabrication technologies advance even beyond optical resolution limits, chip fabrication processes have enabled the design of more complex layouts and architectures, wherein more chip area is applied to pixel and data processing circuitry. Ever more complex processors for image enhancement, display, or more conventional computing tasks can be incorporated in the same display chip without incurring any other fabrication or implementation overhead.

In summary, this new portable display technology demonstrates notable savings in mass, significant reduction in power dissipation, increased display resolution and anti-aliasing technology, compensation for the distortion of simple optical systems for smaller and lighter packages, and the capability to incorporate processing technology directly into the display circuitry. The entire approach for the micro-LCD technology developed under this project leveraged the already existing $100 billion per year interest in silicon processing technology to allow almost immediate implementation of new devices, with greater reliability and very low development and production cost.

2 BACKGROUND

Technology History (previous accomplishments)

Each of the principals for this proposed project has a history of technical accomplishment. As a company that grew out of MIT's technology transfer path, The MicroDisplay Corporation maintains strong historical and current ties to the University laboratories, and continues joint development efforts with MIT and USC. Strong industry support, venture investments, and DARPA technology development contracts form the financial foundation of The MicroDisplay Corporation.

VLSI MicroDisplay Technology

The single accomplishment which is of primary relevance to the now completed Advanced MicroDisplay project, is the suite of technologies that resulted from the VLSI micro-display DARPA grant to MIT's Artificial Intelligence Laboratory which forms the basis for this proposal. Under DARPA funding, Mr. Alvelda and Mr. Knight developed the highest resolution color display ever made. This high-efficiency color display technology was chosen as one of the best technical papers presented at the 1995 Society for Information Display conference in Orlando. This diffraction-based color research was in addition to all of the software CAD and analysis tools development, and the design of the MicroDisplay Compiler for optical compensation.

Support Organization

Starting Organization

Mr. Phillip Alvelda is the founder and Chief Technical Officer of the MicroDisplay Corporation, and was the Principal Investigator for the Advanced MicroDisplay program. As a student at the MIT Artificial Intelligence Laboratory, Mr. Alvelda researched novel computation and sub-micron fabrication methodologies using advanced materials and intrinsic device physics. During his tenure there, he founded the VLSI MicroDisplay laboratory and was the lead investigator for the program under DARPA sponsorship. His editorial responsibilities include peer-reviewing papers for such prestigious journals as IEEE transactions on Neural Networks and ASSP, and Neural Computation and the Society for Information Display Technical Journal. Before joining MIT, Mr. Alvelda was employed in the Neural Computation and Nonlinear Science group at the Jet Propulsion Laboratory where he was responsible for successfully leading the development of the Neural Star Pattern Identification system for Spacecraft Attitude Determination under internal research (and later DARPA) funding. In 1986 Phillip joined the Celestial Sensors group at the Jet Propulsion Laboratory where he redesigned, built, and tested, a second-generation C.C.D star and extended-body target tracking system from electronic hardware, mechanical and vacuum systems, and software control design which has since flown on two space shuttle missions. Prior to his work for NASA's Jet Propulsion Laboratory, Mr. Alvelda received a Bachelor's degree in Physics from Cornell University in 1986.

Mr. Michael Bolotski also received a doctoral degree from the MIT Artificial Intelligence Laboratory before joining the MicroDisplay Corporation. He holds a master's degree in electrical engineering from the University of British Columbia, where his thesis research focused on the design of a massively parallel SIMD computer architecture, ranging from design of CMOS VLSI components to computer vision algorithms. His other fields of research include computer vision VLSI circuit designs, and computer aided design. In industry, he has worked on image processing and graphics software for commercial flight simulators, and on the design of a specialized vector processor for the simulator visual systems. Mr. Bolotski will be the senior VLSI systems engineer and designer for the microelectronics and Silicon Compiler parts of the Advanced MicroDisplay technology project.

Mr. Ramon Olivier is a founding Vice President of The MicroDisplay Corporation and was the administrative point of contact for this project. Mr. Oliver earned a BSEE from Cornell University in 1985. He concentrated in electro-optical devices and microwave theory. In the same year, he joined Rockwell International in the Electro-Optical Center, located in Anaheim, California. As a device physicist, he researched the behavior of electro-optic materials at cryogenic temperatures, designed multiplexor electronics, and pioneered new modeling techniques for the characterization of silicon and mercury-cadmium-telluride infrared sensors.

In 1989, Mr. Olivier left Rockwell to pursue an advanced business degree at the Yale School of Management. He spent one summer interning as an investment banker at First Boston in New York City. In 1991, he graduated from the Yale School of Management and received his Masters in Public and Private Management. He immediately joined V.I. Corporation (now DataViews Corporation) where he was Director of Marketing. He has gained valuable experience in directing a domestic direct-sales force, telemarketing organization, and international distributors. He has also worked closely in forging OEM relationships with major corporations such as Motorola.

Present Organization

Due in large part to the growth enabled under this project, The MicroDisplay Corporation has been enable to acquire numerous employees whose collective experience have greatly added to the company's capabilities. The present organization looks as follows:

Allan Abbott, *CEO*
Phillip Alvelda, *CTO and Founder*
Mike Bolotski, *VP Microelectronics Engineering*
Candice Brown, *Senior Process Engineer*
Imani Brown, *Administrative Coordinator*
Jean-Jacques Drolet, *Senior VLSI Engineer*
Farid Durrani, *VP Manufacturing Operations*
Chris Foley, *Research Engineer*
Kevin Glover, *Electro-Optics Technician*
Madelyn Homick, *Executive Assistant*
David Huffman, *Senior Research Engineer*

Ya-Chieh Lai, *VLSI Engineer*
Nancy Lewis, *Project Coordinator*
Maritza Maldonado, *Human Resources Specialist*
Chris Mullin, *Research Engineer*
Michael O'Brien, *Discrete Electronics Engineer*
Ramon Olivier, *Vice President*
Herman Rodriguez, *Mechanical Technician*
Terri Ross, *Senior Buyer/Planner*
Hongqin Shi, *Senior Research Engineer*
Stephanie Silman, *Marketing Communications Specialist*
Satinder Singh, *VP Engineering*
Rand Stadtman, *Electronic Design Engineer*
Todd Stiers, *Systems Administrator*
Steven Stitt, *Controller*
Carlin Vieri, *Senior VLSI Engineer*
Xiaodong Wang, *LC Alignment Expert*
Tim Wayda, *PC Board Designer*

3 DETAILED TECHNICAL GOALS, RATIONALE, & APPROACH

Detailed Technical Goals

The MicroDisplay Corporation's technical goals

The technical goals for this project were to demonstrate extreme CMOS integration capabilities within MicroDisplay substrates, based on the most current low-power CMOS technology. In detail, the technical goals were to develop both 320x200 and 640x480 active matrix pixel arrays, integrated display row and column data drivers, integrated NTSC, JPEG, and MPEG ASIC decoders, asynchronous serial and RS-170 logic interface, integrated lamp, EL, and LED illuminator drive circuitry, and, through a subcontractor, an integrated programmable microprocessor.

ISI/USC Subcontract technical goals

The programmable microprocessor core portion of this program was subcontracted to the Information Sciences Institute of the University of Southern California. The specific goals of the integrated programmable microprocessor were to design and implement an ultra-low-power microprocessor core with conditional clock-powered logic, a resonant clock driver that can be synchronized to an external clock source, a 1.5V clock-swing compatible latches and drivers, a <1.5 mw core dissipation at 14.3 MHz, and an extended multimedia-type instruction set, named MicroDisplay Extension, or MDX .

Detailed Technical Rationale

MicroDisplay Technology

Liquid-crystal-on-silicon microdisplays (Fig 1) are semiconductor devices that function much like traditional liquid crystal (LC) displays, except that they reflect rather than transmit incident illumination. Instead of liquid crystal material and electronics sandwiched between two pieces of glass as in the laptop display TFT technology, microdisplays are comprised of a silicon substrate with embedded electronics and a liquid crystal layer covered by protective glass.

Since drive and interface electronics are easily integrated with the display on the silicon substrate, a compact device results with fewer interconnects that can eliminate many standard interface chips.

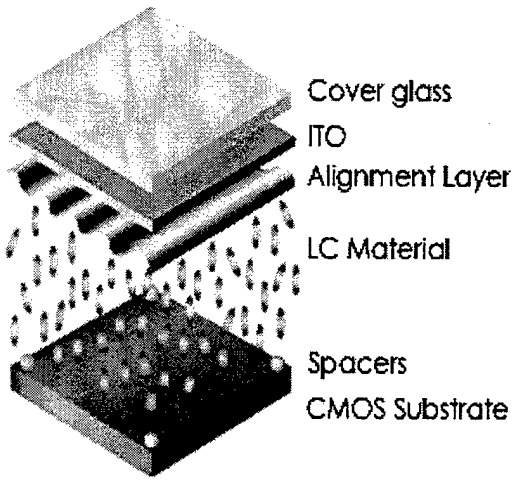

Figure 1- An illustration of a standard Liquid-Crystal-On-Silicon microdisplay architecture, with the glass cover laminated to the CMOS circuit backplane sandwiching LC material in between.

Microdisplay substrates are fabricated in the CMOS process common to semiconductor foundries around the world, so as economies are realized at the foundry level they are applied directly to the production of microdisplays. Microdisplays currently range from 0.25" to 0.9" diagonal with resolutions up to XGA (1024 x 768 pixels) so they fit environments not served by classic LC displays.

Since early 1991, with the founding of the VLSI Microdisplay Laboratory at the Massachusetts Institute of Technology, Mr. Alvelda and, more recently, the entire technical team at MicroDisplay has been working to assemble a complete suite of core technologies necessary to manufacture microdisplays for portable applications in high volume. To date, the Company has recruited a first-class engineering development team that fully addresses the core competencies needed for microdisplay design: microelectronics, PC boards, LC materials, and optics. With more than fifteen design engineers, many with doctorates, this team has produced the most advanced microdisplays in the industry. Today, this portfolio of intellectual property, trade secret, and manufacturing infrastructure is the most complete in the industry. In contrast to several competitors that outsource much of their system design work to third parties, MicroDisplay has assembled all of the key component technologies necessary to maintaining the company's current competitive advantages

Extreme Integration

MicroDisplays are tiny, high-resolution reflected-mode liquid crystal displays. They are based on conventionally fabricated CMOS active substrates laminated with liquid crystal materials. The primary advantage of a single-crystal-silicon substrate is that it is very simple to incorporate high-performance circuitry together with the display device. MicroDisplay has fully embraced the "system-on-a-chip" system design strategy. As performance, portability, and battery power become the critical factors in consumer electronics design, all of the electronic components are evolving towards higher levels of integration. Each generation of portable electronics contains more functionality in each component. Likewise, these portable systems also require display capability. MicroDisplay has developed, implemented, and verified an extensive library of active-matrix pixel array circuit designs and intellectual property that can be embedded in single-chip systems.

In addition, the MicroDisplay manufacturing process leverages the multi-billion dollar semiconductor research and manufacturing infrastructure in the United States. Because the MicroDisplay substrate is based on a standard CMOS process, all of the commercially available and industry-standard microelectronic technology can now be designed to lie alongside the display circuitry on the same substrate. Current MicroDisplay prototypes have demonstrated the integration of active-matrix pixels, LC line-select and data driver circuitry, and simple DRAM, SRAM, and serial shift-register interface circuitry. In this document, we propose to take much greater advantage of the power of CMOS on silicon by incorporating more complex circuit elements on the display die. The following list summarizes several of the communication, computing, and interface circuitry that will be part of the advanced MicroDisplays for portable systems.

Interface and Communication Logic

Previous versions of the MicroDisplay devices relied on wide address and data channels such as SRAM and DRAM architectures for local integration with other discreet components such as microprocessors and flash analog to digital converters. The Advanced MicroDisplays developed under this project, however, incorporate this decoding functionality on the display die. This allows a narrower external communication channel for more compressed data transmission over longer range to consume less network bandwidth. Accordingly, the interface circuits developed for integration into the MicroDisplays conform to industry standards which allow transmission of compressed data as opposed to bitmaps (for example). Initial prototypes include simple ASCII and I^2C serial interfaces, and RGB VGA decoders on the MicroDisplay die with TV tuner modules and micro-controllers mounted on a multi-chip module. Later devices include NTSC and VGA decoders and the next generation will integrate a low-power microprocessors for full-motion video applications.

Microprocessors (Subcontract Technical Rationale)

For a truly programmable display device, there is no substitute for the direct incorporation of a microprocessor or microcontroller. The AC-MOS Group at ISI, who completed this portion of the project, has been conducting research into low-power CMOS VLSI designs for over five years. Prior to this project, their latest development had been a 16-bit low-power microprocessor, named AC-1 (Fig 2). AC-1 was designed under DARPA contract # DAAL01-95-K-3528, *Pulsed Power Techniques for Energy-Efficient Portable and Embedded Computing Systems*. At the user level, this looks like any other microprocessor. However, at the circuit level there is a striking difference. Unlike other microprocessors, AC-1 chips use energy-recovery CMOS to conserve and reuse energy that would otherwise be dissipated as heat. The power savings are a result of how energy is handled inside the chip.

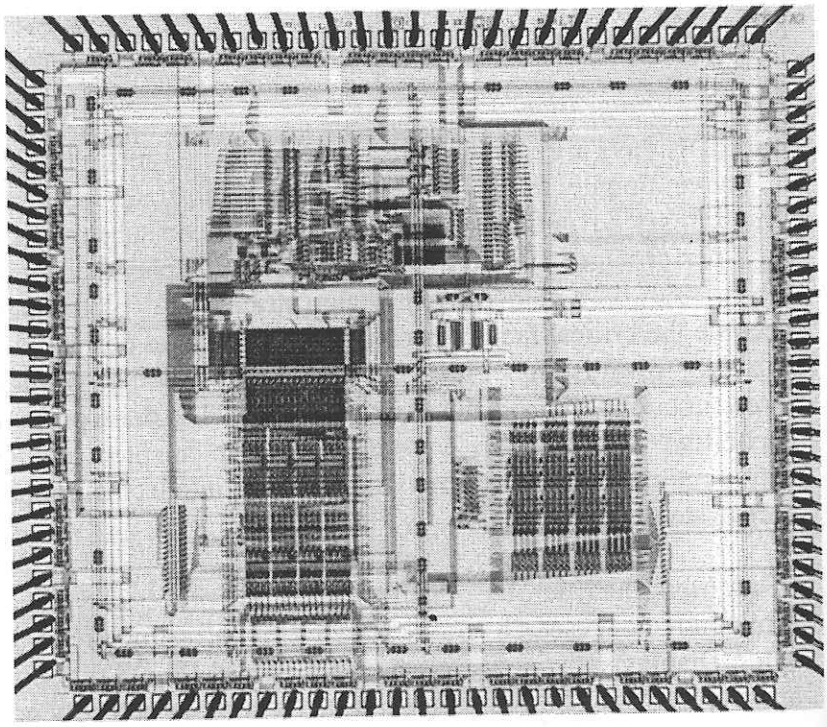

Figure 2– Design layout of the low-power AC-1 microprocessor. AC-1 uses energy recovery circuitry to conserve and reuse energy.

For this contract, ISI proposed to research, develop, and prototype a derivative of their AC-1 microprocessor to be used as an ultra low-power microprocessor with the MicroDisplay LCD prototype system. More specifically, this new chip was designed to feature special instruction

extensions for the byte-wide operations and other special-purpose microdisplay controller requirements. The featured clock-powered logic technology includes balanced (dual rail) clock powered static logic, a stoppable and phase-lockable resonant clock driver, small clock swing compatible latches and drivers, less than 1.5mW core dissipation at 14.31818MHz, an custom instruction extensions.

Low Power LCD Circuits

The dominant power dissipation mechanism in reflective liquid crystal displays is that associated with charging and discharging the parasitic capacitance of internal silicon nodes, and the large capacitance of the liquid crystal cell itself. For low-light viewing conditions, the power load in MicroDisplay devices is almost equally shared between the MicroDisplay and the illuminator. For this reason, we have applied new low-power microelectronic techniques to both essential parts of a portable system.

Low-power MicroDisplay Architecture

From its very beginnings, MicroDisplay development was focused on the low power requirements of portable devices. The first obvious power-saving advantage of MicroDisplay technology is the electronic performance of the single-crystal silicon substrate. Competing technologies such as amorphous or polysilicon on glass displays suffer from large parasitic resistances, poor transistors, and generally slow and inefficient circuit performance. With ever-increasing photolithography resolution, even RF circuitry may be integrated beside active matrix circuits on the MicroDisplay. One beneficial side effect of this high-performance capability is that the power dissipation is much lower than on insulating substrates used in competing technologies.

Another key facet of the low power MicroDisplay architecture is an emphasis on materials that switch at low voltages using smaller cell-gaps. The driving motivation for low-voltage design, the same as in the semiconductor industry at large, is that primarily capacitive CMOS circuit power dissipation is proportional to the square of the driving voltage. The low-voltage nematic materials used in the MicroDisplay devices have switching thresholds below standard CMOS operating voltages at switching time-constants of less than 10ms.

Low-power Virtual-imaging Configurations

One useful observation is that when a display is used in a virtual imaging configuration with a magnifying lens system before it, a display device with a given resolution can then be made much smaller. This means that the total capacitance of the display device (which is proportional to the die substrate area) is much smaller, and the device's power dissipation is correspondingly lower as well. In other words, a portable MicroDisplay in a virtual image configuration can project an image of the same perceived size and resolution as a direct-view display requiring orders of magnitude less power. For example, a $1cm^2$ MicroDisplay using a simple f/2 lens can easily display a 1024x768-pixel image on the user's retina which appears as a 12" monitor 3 feet in front of the user. The power consumption of the virtual MicroDisplay would be almost a factor of 1000 lower than a 12" direct-view liquid crystal display. This means that without sacrificing resolution or display performance, by holding the MicroDisplay close to the eye in

either a pocket pager or pen format, or even an eyeglass clip-on form-factor, battery life can be considerably extended.

This inherent power efficiency of silicon MicroDisplays is also enhanced in the virtual imaging configuration by their proximity to the eye. Since light not striking the retina is wasted light, most light emitted by conventional large format displays is wasted, or worse, provides information to potential adversaries. Square law improvement in effective brightness can be obtained by locating small displays closer to the eye than larger displays remotely located. This means, from a practical standpoint, that LED illumination can be used, leading to high conversion efficiency and high spectral purity in the illuminator. This is an important point for the grating-based color displays as well as greatly reduced overall power consumption.

The reciprocity failure of the human eye is also a potential source for large improvements in illuminator power efficiency. The human eye is well known to be more sensitive to peak illumination than it is to average illumination. We plan to capitalize on this effect by using short, bright illumination pulses from LED illuminators rather than dimmer, continuous illumination available from more conventional light source drive techniques, thereby considerably reducing the illuminator duty-cycle and overall power consumption. This technique is also suitable for driving EL materials for the direct-view monochrome devices at lower power.

Simulator and Compiler Technologies

The increasingly complex set of software tools necessary to design, verify and fabricate silicon circuits and LCD modules are key factors in the success of rapid development projects. A key aspect of MicroDisplay design and fabrication technology has now been implemented to allow unprecedented speed in the implementation and testing of new designs. The MicroDisplay compilers and simulation tools developed under this contract allows simple display specifications to be automatically compiled into almost complete custom designs. Using this new software infrastructure, MicroDisplay was able to demonstrate a complete design, verification, fabrication and testing cycle for four new MicroDisplay designs within two months.

Detailed Technical Approach

Extreme Integration of Displays, Interface, and Communication Logic

The central research issue under the proposed development contract was to determine the feasibility of further integration of portable system electronics within the new MicroDisplay substrate technologies. The new MicroDisplay backplanes could be manufactured using the same CMOS silicon backplanes upon which microprocessors and standard digital logic are fabricated. This means that there is no longer a technology mismatch between the display system components and the computing and communication elements. The remaining question was to determine the optimal level of integration for portable systems in terms of yield, manufacturability, reliability and cost.

The successful demonstration of the contract deliverables has now proved that extreme integration brings extraordinary advantages. The NTSC / VGA decoder die described below unequivocally demonstrates the advantages of this approach:

1.) **Display device yields and costs** are not significantly affected by adding extra peripheral logic. The addition of all the VGA and NTSC decoding logic increased the microdisplay area by less than 7%, even using an older 0.8 micron CMOS process. Using a state-of-the-art 0.18-micron process the added are could be less than 2%. The added cost of this extra area is negligible compared to the rest of the accrued advantages below.

2.) **Parts count and silicon cost** is substantially reduced with fewer active die. The additional parts do not require assembly, integration, packaging or testing.

3.) **Packaging size, complexity, cost and reliability** are all improved with fewer components and simpler interconnections. The result is smaller, more portable products with greater lifetimes.

4.) **Power consumption** is also minimized with the elimination of external packaging parasitics between active chips. In a single-chip device, there are no external bond wires, chip packages, or PC-Board traces to drive. The power consumption thereby drops by an order of magnitude, as demonstrated by the NTSC / VGA decoding microdisplay described below.

5.) **System Interface** is also significantly simplified when on-chip decoding logic can decompress data provided to the single-chip system over a narrow interface with few wires. For example, the MicroDisplay NTSC/VGA integrated decoder had a four wire interface to an NTSC source, rather than the 18 wire interface of a "raw" display without decoding logic.

The research and development effort for the integrated microelectronic circuitry was a low-risk effort in standard electronic VLSI design technology to design interface and control logic for the active-matrix display elements. All of the proposed electronic elements were historically very well understood and, in the cases where they are commercially available, were be directly integrated. The efforts concentrated on integrating tiny elements of the smallest possible area necessary to control and interface to the display, and refining layout techniques for optimal packaging, and yield. The low-power circuitry involved extensive research, not only in the CMOS SCRL logic design for drive and control circuitry, but also characterization of appropriate circuit parameters based on LC materials properties. These experiments were carried out through the sub-contract with ISI.

The preliminary phase focuses mostly on those subsystem technologies which appear most promising, and consists of two main parts: (1) theoretical analysis and computer (SPICE) simulation experiments on real data and circuit designs, and (2) fabrication of several prototype CMOS display circuit elements for integration and performance evaluation experiments.

Microprocessors (Subcontract Technical Approach)

Power is the rate at which physical energy is exerted. The conventional microprocessor dissipates energy primarily in short bursts that occur when the clock lines switch from high to low voltage, or vice versa. Hence one immediately apparent method to reduce power dissipation is to lower the clock frequency. This will reduce the power but also the computing speed. The

computation will take the same amount of energy but since the energy is delivered at a slower rate, the power is lower. For a battery-powered system, the total battery drain is the same whether the computation takes a long time or a short time. The real goal then is to develop a low-energy microprocessor that will reduce the total battery drain for the same computation.

The situation is counterintuitive. The computation *should* take less energy if we are willing to increase the computation time (i.e., wait longer for the result). The most common technique used to trade-off computation time for energy is called "supply-voltage scaling." With this technique, energy dissipation is reduced by decreasing the voltage swing of the signals. The scalability of this approach is limited to the threshold voltage of the transistors. The circuits become extremely slow when the supply voltage is near the threshold voltage. It is possible, at the CMOS-foundry level, to reduce the threshold voltage, but there are other process and circuit problems with this approach. Typically CMOS circuits have very small power dissipation when the circuits are idle. As the threshold voltage is reduced, the idle (or static) power dissipation increases exponentially.

Energy-recovery CMOS is a relatively new technique that does not share the scalability limitation of supply-voltage scaling. It is based on a result from computational thermodynamics. Slowing down the speed of energy transport can reduce energy dissipation. The energy that would otherwise have been dissipated can be recovered and reused from clock cycle to clock cycle.

In the AC-1 microprocessor, the clock circuits do double duty. They perform the regular functions of a clock in a microprocessor, but they also provide the means for extrinsically controlling the speed of energy transport. A first result is that power dissipation due to the clock lines is greatly reduced (more than a factor of 10 in the first implementation). To further reduce energy dissipation, special circuits, called clocked buffers, tap the clock lines for power to drive many of the data and control lines of the microprocessor. Not all of the energy is recoverable and the fraction of the energy that goes into the actual circuits that perform the various logic functions is mostly not recovered. Fortunately, an important fact about real CMOS microprocessors is that much of the power dissipation is due to getting the energy to the places where the bits are computed and not due to the actual switching or flipping of the bits where the computation happens. Simple calculations for modern microprocessor technologies show that the energy required to flip a bit is on the order of femptojoules (10^{-15} joules) while the entire microprocessor may dissipate hundreds of nanojoules (10^{-9}) per clock cycle. This is a difference of seven orders of magnitude. In the AC-1 microprocessor we used this fact to our advantage. The clocks power only about 10% of the total number of circuit nodes but the clock power accounts for 90% of the total power dissipation.

From testing and measuring AC-1, we have been able to experimentally determine that energy recovery works in CMOS and can be used to significantly reduce power dissipation. To prove the effectiveness of the *clock-powered* approach, we built into the AC-1 microprocessor two complete clock circuits. The first is a conventional clock circuit that works by the conventional rules of dissipating all the input energy. The second is an energy-conserving clock circuit that recovers and reuses energy via inductors. An external pin selects which clock circuit is engaged. The difference between the conventional clock driver and the energy-recovery clock driver ranges from a factor of four to five in the frequency range of 35 MHz to 54MHz. Although, only

10% of the circuit nodes are powered by the clock, but these nodes account for most of the power dissipation. From measurements for the conventional clock drive mode, the clock power was approximately 90% of the total power.

Low-power MicroDisplay Architecture

Part of our effort has been devoted to the development of a previously unknown multiple input NOR structure in CMOS that is faster than competitive gates when the number of inputs range from 2-40. The gate uses source follower NMOS devices in a parallel arrangement driving the P pull-up at the same time a parallel array of N devices pulls down. While dissipating sufficient static power to be unattractive for use everywhere in a design, the selective use of this circuit sped up critical paths in PLAs, decoders, comparators and wide selectors. We have developed techniques for ameliorating the severe noise behavior of modern CMOS components. A custom clock driver, for example, drastically reduces on-chip power supply noise by intentionally dissipating static power in the clock driver during static periods of the clock, such that the current drawn during the transitions remains approximately the same as the static power. Another approach utilizes coding theory to eliminate data dependent noise in wide data busses by equalizing the number of zeros and ones in the data word. It requires only log N additional data bits, and has a fast (log N) implementation. An active area of our research has centered on the development of low power pads for our circuits. This is an essential aspect of the technology, since high performance requires terminated transmission lines, and terminated transmission lines normally require high power drivers. The pads we have developed utilize a low-voltage driver that makes use of the parasitic resistance of the driver transistor as a series termination resistor. The resistance of this driver is digitally controlled, and is under control of the on chip boundary scan circuitry. By watching the reflections on this series--terminated line, we can determine and compensate for both the line impedance and the line delay. By noting the impedance vs. distance function, we can evaluate the high frequency integrity of the strip-line wiring in addition to the normal DC continuity measurements allowed by boundary scan techniques.

Optics

The efforts in electronic and LCD investigation were paralleled by preliminary research in simple optical systems for use with the micro-electronic display technology. Preliminary experiments in optical systems resulted in several promising single-lens architecture MicroDisplay systems. Additionally there are certain aspects of designing display optics for each of the various form-factors (pen, watch, pager, etc.) which needed to be carefully selected and optimized. These factors concerned issues such as field-of-view, aberration, coma, optical path-length, chromatic aberration (for color displays) and were addressed using state-of-the-art MicroDisplay optical design software tools and analytical methods.

Facilities

The MicroDisplay Corporation is headquartered in the San Francisco Bay area, in close proximity to major semiconductor suppliers as well as a large number of customers. The West Coast location is conveniently located to cover both U.S. and Asian markets. The initial MicroDisplay facility will consist of adjacent office space, laboratory, and clean-room manufacturing space suitable for the pilot-line equipment described above.

Strategic Technical Plan

Overall, the risk associated with each sub-component of the Advanced MicroDisplay Technology research and development program has been rather low. The actual integration of what heretofore have been considered disparate technologies into a single novel and incredibly useful display device is what constitutes the main body of risk and research. Considerable research was applied to determine the best evolution of each of these separate disciplines towards a useful marriage. Applications range across any portable system which conveys data, from watches and calculators, to diagnostic tools, to vision enhancement, to multi-sensor fusion devices. In particular, understanding concepts stemming from the marriage of Liquid Crystal technology with high-performance CMOS VLSI logic and our present semiconductor device fabrication ability would promises even further advances portable systems technology across the display industry.

MicroDisplay plans to leverage those technologies that are well established in the US and to concurrently investigate the customization of each of these electronic, optical, and display technologies for micro-sized display devices. Further, the integration of CMOS and Liquid Crystal technology in particular provides a foundation for follow-on development of next-generation holographic displays. MicroDisplay has also leveraged its university and industry ties through subcontracts with USC and MIT for low-power CMOS circuit design. The development project began with an Initial Research and Design and Interface Standards Specification phase. This phase continued at a diminished level throughout the development cycle to insure the smooth integration of the various subsystems. The initial research phase also began the negotiations with subcontractors for the eventual fabrication of custom materials and sub-circuits to be integrated at the MicroDisplay Facility.

After the baseline requirements and standards were established, a concurrent cooperative effort was targeted develop appropriate VLSI electronic, Optical, Display Media, and Mechanical design components of the entire microdisplay system. Toward the end of the independent design phases, the subsystem integration effort began to coordinate more closely the efforts of the subsystem design teams, and selected sources were chosen to supply either materials or fabricated subsystems as appropriate. When the microdisplay Research and Development project was complete, all of the necessary material and device resources and technology were in place, ready to immediately begin large-scale production of Micro-displays upon receipt of private funding agreements.

Collaborations

ISI/USC

MicroDisplay's collaboration with the Information Sciences Institute of the University of Southern California had been very productive. The resulting low-power microprocessor technology development has also resulted in synergistic developments of low-power LCD drive electronics both at MicroDisplay and at USC. These new developments will have broad application over the entire display industry in addition to their direct use in microdisplay systems. MicroDisplay's collaboration with USC/ISI is expected to continue with future government contract and commercial ventures.

MIT and Berkeley

MicroDisplay also maintains strong ties with the low-power electronics design groups at MIT and Berkeley as well as the Sloan School Entrepreneur Center. Both schools have provided world-class design and business talent for developing and commercializing new embedded system technologies.

4 RESULTS

Project Deliverables

The primary deliverable resulting from this program is the Advanced MicroDisplay technology, which consists of the materials, software, microelectronic, optical, mechanical, interface, and manufacturing research and development required to fabricate portable MicroDisplays for commercial and government applications. This technology has been validated by the development of prototype hand-held video display devices with the integration of appropriate optical, mechanical, control and electronic interface components to provide a proof-of-concept test-bed suitable for further technology development.

In Particular, the Target deliverables consisted of:

1. Detailed Technical Reports
2. Black and White MicroDisplay with:
    - Video Resolution Black and White Active Matrix Circuits
    - LC Drive Electronics
    - Black and White NTSC Video Decoding Circuitry
3. Universal Programmable MicroDisplay
    - Video Resolution Black and White Active Matrix Circuits
    - LC Drive Electronics
    - Integrated PIC-style 8-bit CMOS micro-controller
    - Asynchronous serial command bus
    - I^2C Data-bus interface
4. Prototype Advanced MicroDisplay Systems

There are no proprietary claims by any third party on the ideas of products for this project. The MicroDisplay Corporation and the researchers named in this document have full control over all intellectual and material rights.

With respect to any subject invention in which the Contractor elects to retain title, the Federal Government shall have a nonexclusive, nontransferable, irrevocable, paid-up license to practice or have practiced for or on behalf of the United States the subject invention throughout the world.

Project Results

Technical Reports

Thorough documentation of these technologies has been provided as a set of weekly and monthly technical reports. The reports have covered specific system issues concerning prototype development and detail progress in technology development and integration.

Grayscale MicroDisplays

Gray1

The early Gray1 display is a monochrome display with a 512 x 300 resolution. It features a complementary pass-gate pixel design (Fig 3). The narrow poly buses increase gate signal rise time and therefore decrease charge injection. The pixel side of the pass transistors has extended diffusions to increase capacitance. The pixel capacitance is shielded on the first metal layer from the vertical column wire by a ring of metal connected to a power pad. The second metal ground plane connects to the substrate to provide a low-impedance ground plane.

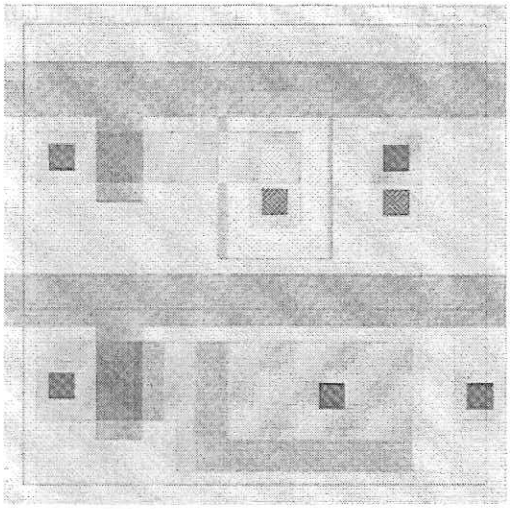

Figure 3 - A schematic layout of the Gray 1 display pixel. The different colors correspond to different CMOS circuit layers. The key innovation is the continuous ground-plane/light shield shown in purple. This almost continuous layer protects the pixel transistors from light leakage and also improves the electronic performance and noise immunity of the pixel array.

Gray2

The Gray2 (Fig 4) display is an active-matrix display with a 640 x 480 resolution. Integrated horizontal and vertical shift registers reduce driving logic. The device is easy to interface, requiring only a single analog video input and six digital inputs. The line timing supports interlaced and non-interlaced scanning, as well as windowing of a larger virtual display. Rows and columns are driven sequentially in raster order. The display supports externally generated, and therefore, arbitrary inversion patterns, including frame, row, column, and pixel inversion. Additional features this display incorporates include a 1.8-Volt analog video input and ultra-low power consumption (30mW total power consumption, worst case).

From a digital point of view, a Gray2 display consists of an array of pixels and two shift registers. The horizontal shift register controls the column lines, while the vertical shift register controls the row lines. The horizontal shift register output controls which of the columns is connected to the video input. As the horizontal shift register is advanced, each successive column samples the video data via a track-and-hold

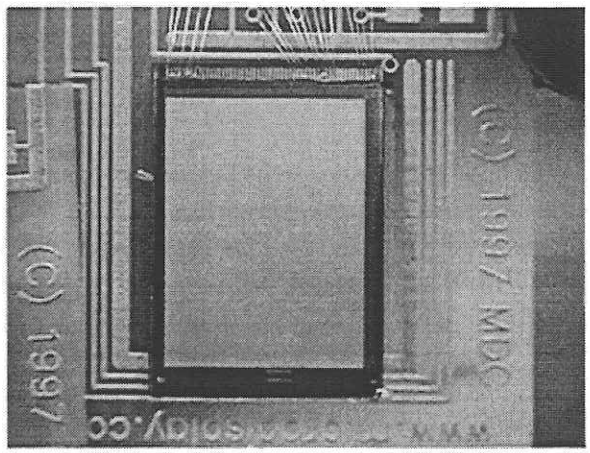

Figure 4 - A close-up of the Gray2 display bonded to a display carrier shows the minimal space required by the chip's integrated circuitry. More than 95% of the chip real estate is dedicted the display's pixel array.

mechanism. The column line tracks the video line voltage at the start of the pixel interval and maintains the voltage after the switch is turned off at the end of the pixel interval.

After the columns have sampled an entire video line, the pixel voltages are transferred to the pixels of the current row in the pixel array, as selected by the vertical shift register. The LOADROW pulse initiates the voltage transfer. After the voltage transfer step, the vertical shift register is advanced, selecting the next line, and the sampling process starts with the next video line.

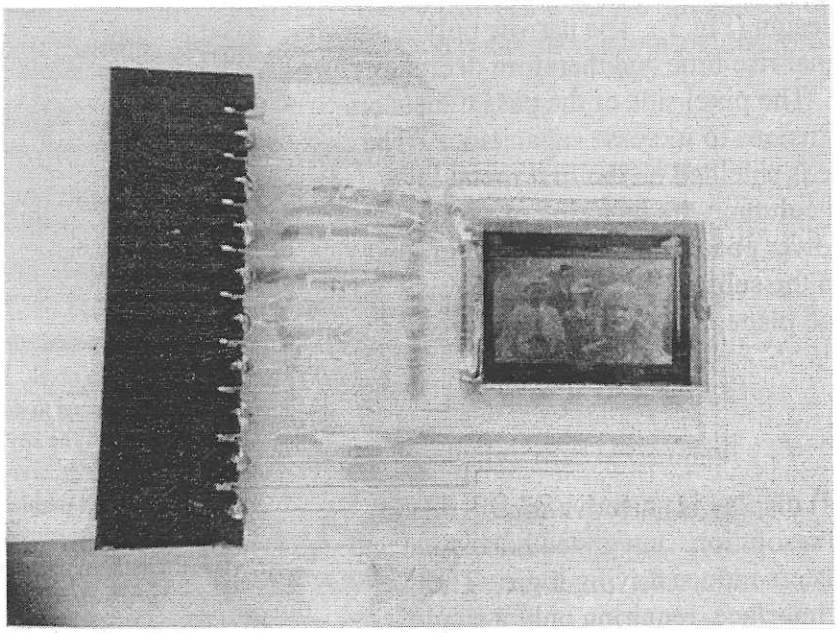

Figure 5- The Gray2 MicroDisplay operating in direct view with no custom illumination. This "wristwatch-video" mode is the only microdisplay capable of showing full-motion video under only ambient illumination.

The chief innovation in the liquid crystal materials technology for Gray2 was the development of a high-performance LC mode with high contrast and wide viewing angles (Fig 5). In combination with properties of the CMOS metalization properties of the backplane, the result was a MicroDisplay that could be viewed with excellent contrast under ambient illumination. With the elimination of any power dissipation for daylight use, one of the most significant power drains on a personal display system was virtually eliminated.

Universal Programmable MicroDisplays

The MTV-1 Integrated Single-chip NTSC and VGA Monitor

Based on standard reflective display architectures from previous generations, the MTV-1 (Fig 6) display demonstrates new levels of circuitry integration and requires no additional assembly or processing steps. In fact, the new integrated display almost entirely eliminates the need for external circuitry and additional components common to other display systems.

The MTV-1 CMOS substrate includes integrated mixed-signal NTSC and VGA decoding circuitry, as well as liquid crystal drive circuitry, placed alongside a 640 x 480 resolution active-matrix pixel array. This display architecture marks the first complete single-chip display system. The first prototype of this design was fabricated using the Hewlett-Packard 26B 0.8-micrometer CMOS line. The chip diagonal is approximately 0.5", demonstrating that integration does not demand increased chip area. Requiring only power and video signal inputs, this miniature information display is mounted on a small carrier board (Fig 6) that accommodates just the display itself, a power and signal connector, a clock crystal and potentiometers for black level and gain adjustments. The entire system typically runs on a power budget of less than 50-milliwatts and requires no auxiliary driver boards for product integration.

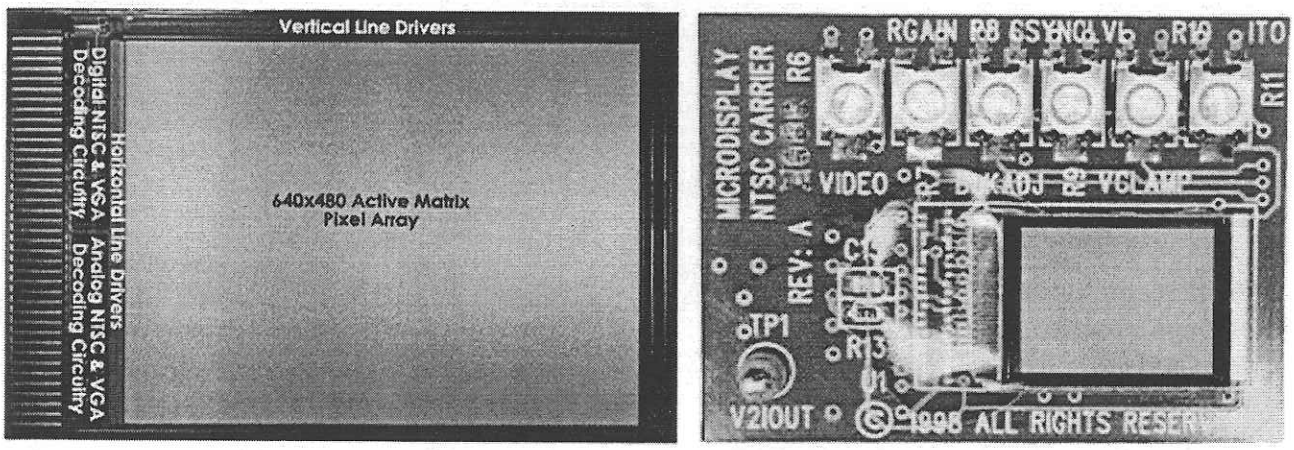

Figure 6 - A photograph of the MTV part, the industry's first "smart" microdisplay complete with integrated NTSC and VGA decoders. All NTSC active components are on the microdisplay die.

This first generation single-chip monitor is suitable for both direct view and projection applications. The successful completion of the single-chip monitor demonstrates for the first time the ability to fully integrate not only the decoding and display driving circuitry into the display backplane, but signal-conditioning electronics, microprocessors, and memory as well.

As design tools advance and silicon foundry fabrication processes permit layouts of increasingly greater complexity, MicroDisplay devices will incorporate progressive levels of functionality without incurring substantial die size increases or additional fabrication and implementation overhead. Moreover, high levels of integration translate directly into reduced power consumption and packaging cost. The MTV integration effort has reduced the grayscale system

power consumption of a high performance display system from over 1 Watt to less than 50 milliwatts.

Additional Display Integration Technology

The Color NTSC Decoder Prototype

Once the integrated MTV-1 chip was developed and tested (a single-chip) Grayscale NTSC and VGA monitor) the next step on the development path was to develop a similar integrated display that would decode and display full color signals. The NTSC Color Board (Fig 7) was designed as a prototyping environment to develop the Digital Signal Processing circuitry for integration of the color decoder on the microdisplay backplane. The prototype board, pictured below, was completed as part of this contract and was used to successfully demonstrate MicroDisplays implementation of the latest DSP code and circuit designs for color NTSC decoding to generate RGB data suitable for direct full-color video display on a MicroDisplay device.

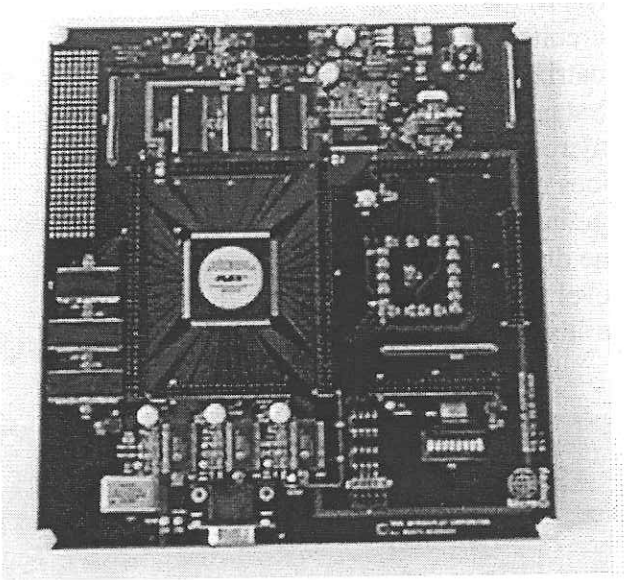

Figure 7 - A view of the first generation NTSC decoder board, which decodes the color information generted from NTSC source in order to drive a monochrome display with red, green, and blue color data.

Fundamentally, an NTSC signal is composed of 3 components: timing data, luminance data, and color data. Separating the timing is very straight forward, as all timing information is transmitted below a certain threshold. Hence, it can be "stripped" off very easily using a comparator. Luminance data is simply the amplitude of the signal, which can be fed directly into our microdisplays to produce a grayscale image.

The color data, on the other hand, is modulated or "encoded," requiring color demodulation or "decoding" by the receiver. This is the major difficulty of any NTSC receiver system. The way this board operates is by first separating the NTSC signal into its basic components, timing, luminance, and chrominance, through the use of digital comparators and filters. Following separation, the chrominance is demodulated into its "in-phase" (I) and quadrature (Q) components. Following this, the I, Q, and luminance or "Y" component, are directly converted into R, G, and B through simple mathematical equations. This digital R,G, and B information can then either be left in digital form, buffered up, and sent to a monochrome display to run in field sequential color mode, or it may be converted into analog R,G, and B passed directly on to a diffractive or reflective color microdisplay.

Now that this color video decoding circuitry has been designed and verified in an ALTERA FPGA device, the programmable logic circuitry can very easily be converted into a custom ASIC design for integration with future MicroDisplay systems.

The MD-1 Low Power Microprocessor

The MD-1 microprocessor (Fig 8) is the result of MicroDisplay's joint effort with the Information Sciences Institute of the University of Southern California. As discussed above, the design for MD-1 was based on an earlier design with several major improvements, which include new register cells, new read-out cells, a single-railed data path, a single-railed control path, a set of 38 basic instructions (similar to Intel's instructions set), 20 additional MDX (MicroDisplay eXtension) instructions for multimedia support, and shared existing functional units for minimized power dissipation.

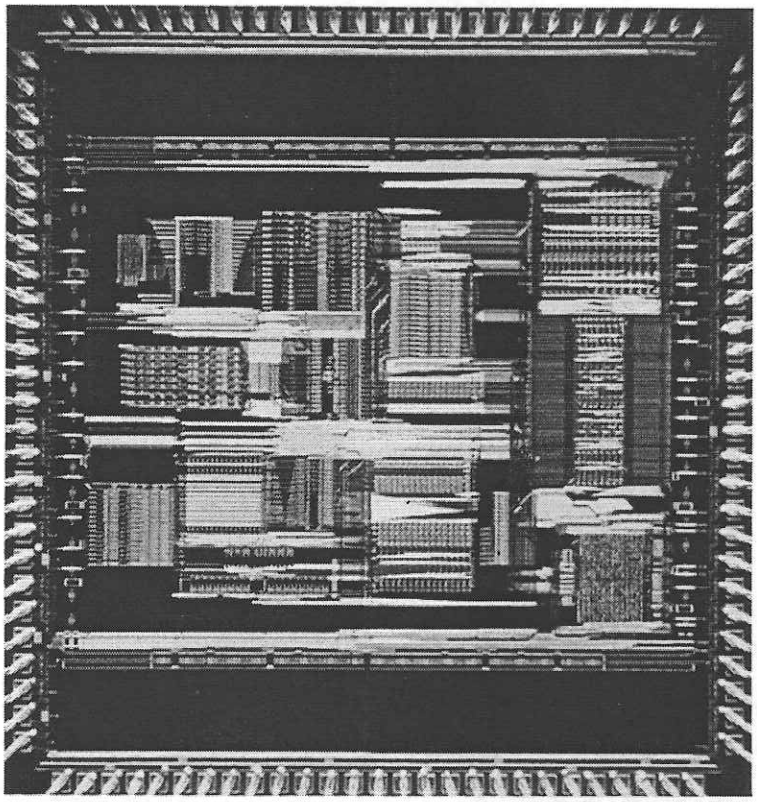

Figure 8 - A magnified top-view of the MD-1 microprocessor chip.

Resulting Optics

The LookingGlass™ Eyepiece

MicroDisplay designed the LookingGlass eyepiece (Fig 9) to provide a prototype viewfinder to aid in the evaluation of its MicroMonitor displays, while keeping the concerns and challenges of the design engineer in mind, such as brightness versus power tradeoffs. LookingGlass operates in conjunction with the Gray2 display and magnifies the 0.5 inch diagonal display so that it appears a to be an 8 inch diagonal virtual image at a distance of 24 inches from the eye. When viewed with the LookingGlass, the Gray2 display has a luminous intensity of 70 cd/m2, approaching the brightness of white paper under a normal reading light.

LookingGlass also provides for a large eye relief, allowing the user to hold the viewer up to four inches away from the eye, for comfort and ease of use. Even with this comfortable eye relief, the LookingGlass provides a field of view that measures approximately 19 degrees in diagonal. In addition, the small, lightweight viewer consumes less than 15mW to power the led illuminator, adding very little to the overall power budget of the system.

The MicroDisplay LookingGlass is constructed almost entirely of plastic injection-molded parts including the single-lens magnifier, the illumination system and the eyepiece package, emphasizing low-cost parts and a low parts count and simple assembly. This will facilitate transition into a wide array of consumer products. In other words, the LookingGlass was designed for ease of manufacture and technology transfer to commercial products. The LookingGlass viewfinder delivers a simple optical reference design that can easily be incorporated into existing products and also opens the way for new generations of products that can take advantage of miniature displays.

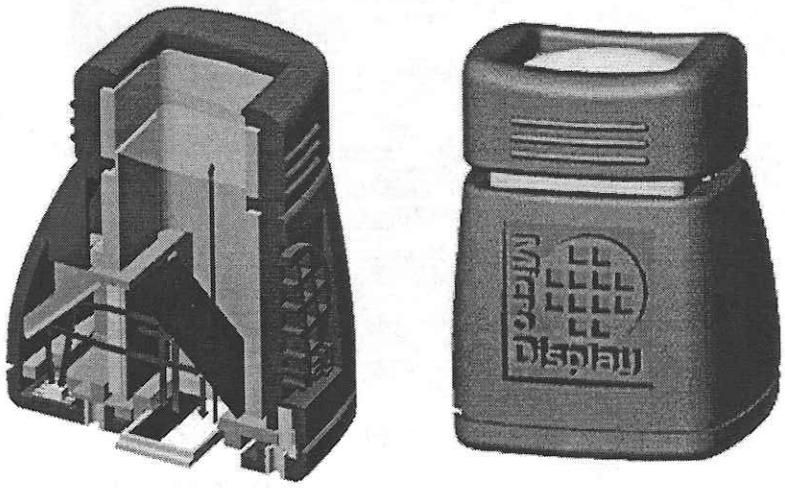

Figure 9 - A detailed cross-section of the LookingGlass optical systen and the exterior design.

Resulting Diffraction-based Color Filter Technology

The original Diffraction-based color filter technology was developed at and licensed from the Massachusetts Institute of Technology. The major effort relating to the diffractive color filters in this project focused on improving the manufacturability of the diffraction gratings in a standard foundry's CMOS process. Original designs suffered from sensitivity to lithography errors that made consistent high yield manufacture of the grating structures impossible. The new grating designs undertaken in this program demonstrated substantial improvements in uniformity and robustness of manufacture using a 0.35-micron 3-metal CMOS process (Fig 10).

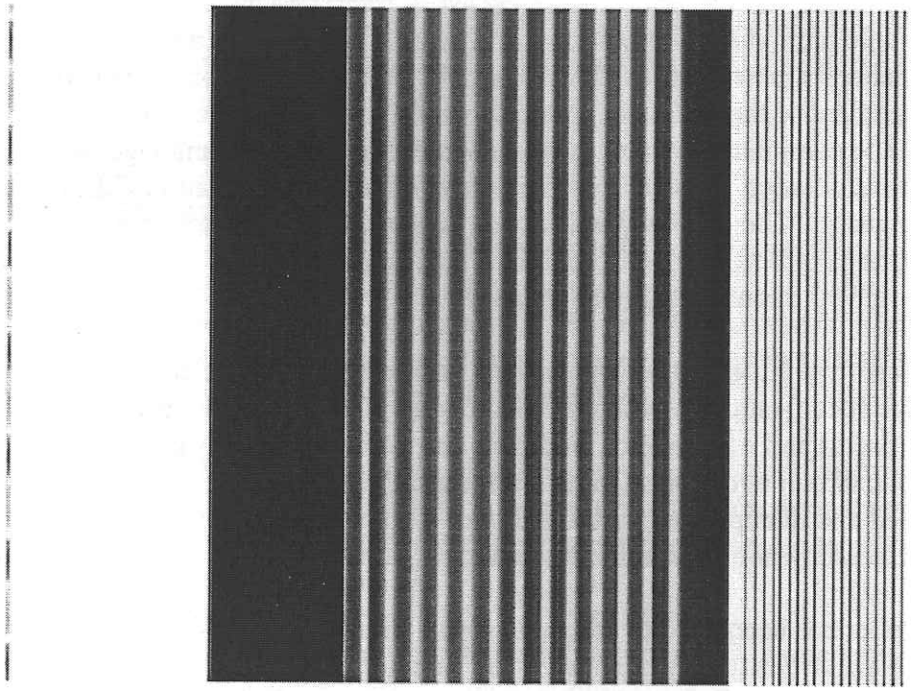

Figure 10 - Shows an SEM Photo of a Blue, Red, and Green grating triad successfully fabricated using a 0.35 micron 3-metal CMOS process. Note the sharp edges and excellent lithography results. (Metal vias betweeen grating legs are as designed.)

Additional work performed outside this contract effort has resulted in the successful development of a QVGA resolution (320x240 pixel) display using the above described new diffraction grating design to generate very high quality color. The QVGA "Rainbow" display was a raw display which included only the diffraction-based color active matrix pixel array, and integrated row and column driver circuitry. A simple external driver board incorporated the same VGA decoding circuitry that was already embedded within the MTV-1 single chip monitor with the minor change of replicating the analog Grayscale driver circuit three times, once for each of Red, Green, and Blue Video signals. The driver board was shown to perform at frame rates of over 200 Hz. The Rainbow display has since been demonstrated in both eyepiece and projection configurations, and promises to significantly simplify system electronics by eliminating the need for a frame buffer in many applications. The optics can also be simplified,

particularly in projection engines to enable a series of truly man-portable projectors for command and control applications. The entire prototype projector's optical system fit inside an 8" x 3" x 1" area and promises real portability in later generations.

Resulting Tools

DisCo Tech Display Compiler Results

The MicroDisplay display compiler technology (DisCo Tech) was developed under this contract specifically to enable rapid display prototyping. The compiler accepts a structural description of a chip; a list of manually generated low-level leaf cells, and a set of geometrical constraints that specify the arrangement of the leaf cells. It produces a final integrated circuit layout that is ready for fabrication. The compiler is written in the Scheme programming language, which is currently under consideration as the standard Electronic Design Automation (EDA) customization language. The display specification is also written in a Scheme syntax, which allows small programs to be easily embedded into the specification. Thus, the compiler can be extended by the user for circuit-specific applications.

The compiler is a software tool that accepts a very detailed display specification including resolution and size specification to produces final layout in conjunction with a human designer. It is intended for use as part of a suite of modeling and verification tools that includes process modelers, symbolic circuit equation solvers, circuit simulators, and layout verifiers and can be interactively varied and manipulated by the designer to generate designs very quickly. The compiler was deliberately not made fully automatic in order to maintain design flexibility.

The display compiler has been used to assemble seven chip designs to date, of which five have been fabricated. All five designs demonstrated full functionality in the first silicon pass. The flexibility of the display compiler was used to design and customize four chips in a four-week interval. The user-extensions allowed designers to change the pixel size several times through the process without manual modification of the surrounding drive circuitry. Other applications of this flexibility included modifying bond pad locations to improve circuit board efficiency, adding a bi-directional capability, and optimizing global wires for speed and power.

Liquid Crystal Behavior Modeling Software

The first logical step towards a better understanding of the possible behaviors of liquid crystal displays, was a materials simulator for experiments in liquid crystal physics (Fig 11). The actual topology of defects in liquid crystal alignment and how they would affect the optical quality of displays is impossible to solve in closed-form for realistic 3-D pixel and grating

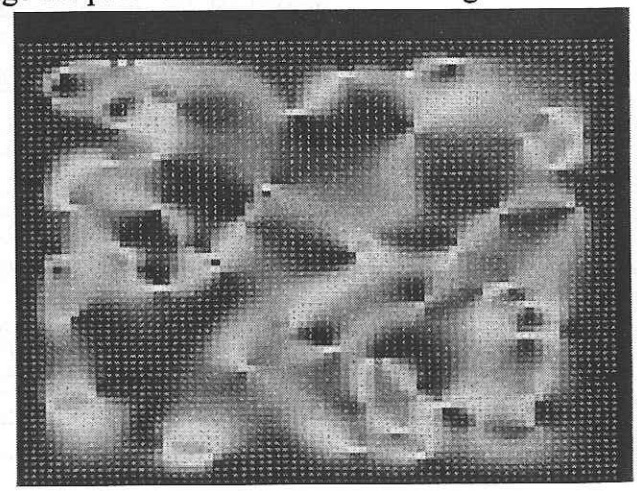

Figure 11 - A 2-dimensional slice of the liquid crystal orientation field in a quasi-relaxed volume of simulated E7 material from BSH.

structures. For some time, there has been a general realization in the field that the most recent two-dimensional simulations failed to capture the full ensemble of defects observed in real three-dimensional volumes of liquid crystal materials. This MicroDisplay software tool simulates a full three-dimensional volume and surrounding electrodes using a complete tensor orientation description of electro-mechanical liquid crystal interaction.

The simulator has three major components. An iterative Laplace's equation solver determines electric fields due to pixel voltages applied at the edge of the liquid crystal volume and incorporates local perturbations to the calculated field from the effects of oriented liquid crystal molecules. A successive over-relaxation module solves for the liquid crystal molecules' local orientation configurations given the electric field determined by the Laplace solver module. Finally, an optical simulator, which is an approximation to Maxwell's equations, simulates the propagation of light through the liquid crystal volume.

Liquid Crystal Continuum Theory

The liquid crystal dynamic relaxation module is based on the continuum theory of liquid crystal relaxation first proposed by deGennes[3] and latter amended by Haas[4] and Kilian[5] for computer simulation in two dimensions. This new simulation test-bed incorporates the latest continuum-theory, extends it to a three dimensional liquid crystal volume, integrates an electric field solver, and performs optical analysis of equilibrium configurations.

The continuum theory of liquid crystal mechanics begins with the development of a tensor description of liquid crystal orientational order. As mentioned above, simple vector field descriptions take into account neither the inversion symmetry of nematic molecules nor higher order anisotropic interactions.

As an example, this description will begin with the definition of a 2-D orientational order matrix for simple rods, and then extend the matrix to more complex shapes using a higher dimensional tensor. This tensor effectively parametrizes how a particular liquid crystal molecule will tend to affect its nearest neighbors given an externally applied electric field. So the order tensor is an operator on the 3-D orientational vector-field. Note that the elements of the order tensor can actually be determined through physical experiments.

A Description of Simple Rod Orientation

The orientation of simple rods has complete cylindrical symmetry about **a,** the molecular axis).

$$a_x = \sin\theta\cos\phi \qquad a_y = \sin\theta\sin\phi \qquad a_z = \cos\theta$$

One can then describe the state of alignment of the rods by a distribution function $f(\theta,\phi)d\Omega$ around the direction (θ,ϕ) (Fig 12).

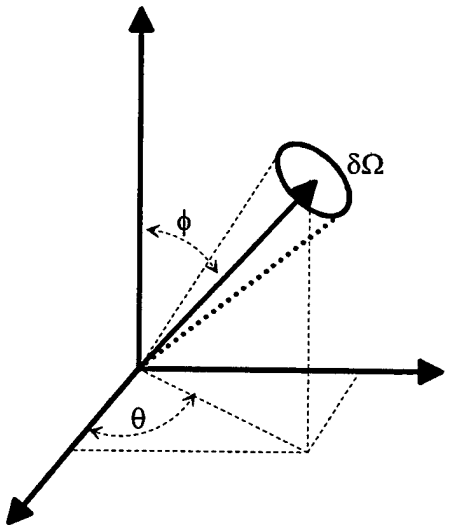

Figure 12 - The spherical coordinates used for the description of rods.

A one-parameter description of orientation might then be the thermal average

$$\langle\cos\theta\rangle = \langle a\cdot n\rangle = \int f(\theta)\cos\theta d\Omega$$

But from the nematic symmetry properties

1.) f is independent of ϕ (cylindrical symmetry about $\boldsymbol{n}$)

2.) $f(\theta)=f(\pi-\theta)$ ($\boldsymbol{n}$ is equivalent to $-\boldsymbol{n}$)

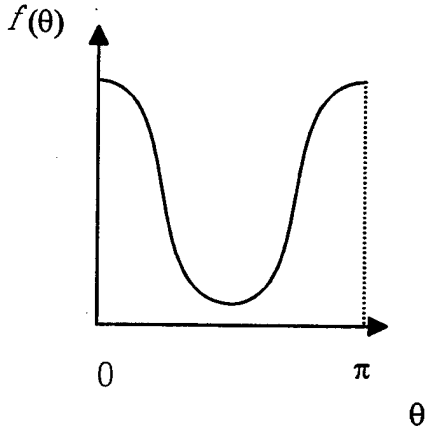

Figure 13 - A typical angular distribution function around the director.

and this simple parametric description vanishes due to symmetry property 2. There is no average dipole, so we need to resort to higher multipoles. The first non-trivial one is the quadrupole moment,

$$S = \frac{1}{2}\left\langle\left(3\cos^2\theta - 1\right)\right\rangle = \int f(\theta)\frac{1}{2}\left(3\cos^2\theta - 1\right)d\Omega$$

For this description, $f(\theta)$ is strongly peaked around $\theta=0$ and $\theta=\pi$ (parallel alignment) $\cos(\theta) = -1$ or $+1$ and $S=1$. If the orientation is random, where $f(\theta)$ is independent of θ, we would have $S=0$ (Fig 13). In this manner, S is a measure of alignment.

For Molecules of Arbitrary Shape

Let **a**, **b**, and **c** be three orthogonal unit vectors linked to the molecule, you can then generalize the notion of an alignment measure ***S***, from above, to

$$S_{ij}^{\alpha\beta} = \frac{1}{2}\left\langle 3\hat{i}_\alpha \hat{j}_\beta - \delta_{\alpha\beta}\delta_{ij} \right\rangle$$

where α and β = x, y, and z, are indices referring to the laboratory frame, while i,j = **a**,**b**,**c** and the δ's are Kronecker symbols. i_α and i_β are the projections of the unit vectors i and j onto the α and β basis. Again, the brackets represent a thermal average (Fig 14).

This new tensor form of S is symmetric in ij and also in $\alpha\beta$. It is also traceless in that

$$S_{ij}^{\alpha\alpha} = 0 \quad and \quad S_{ii}^{\alpha\beta} = 0$$

where repeated indices imply summations. From the previous page, nematic materials have almost complete rotational symmetry about the optical axis. This implies that

$$S_{ij}^{xx} = S_{ij}^{yy} \quad and \quad S_{ij}^{xy} = 0$$

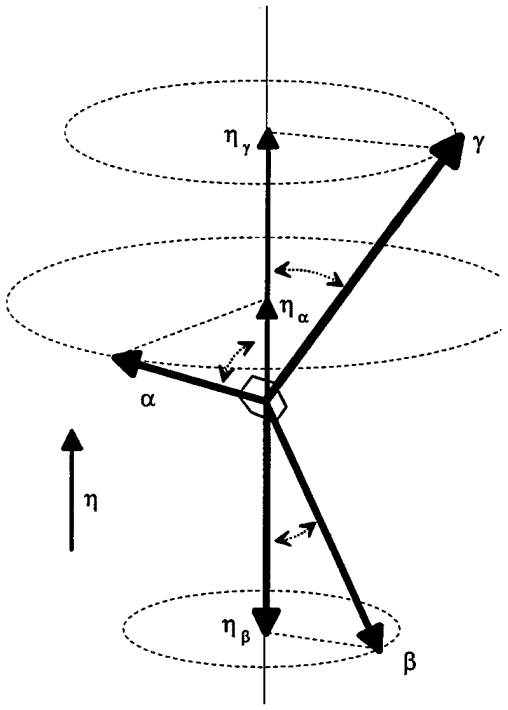

Figure 14 - The projection of the molecular axes onto the local average director η.

Furthermore, since the xy plane is a reflection for a nematic molecule we realize that

$$S_{ji}^{zx} = S_{ij}^{zy} = 0$$

This means that the only non-zero components of S are

$$S_{ij}^{zz} = -2S_{ij}^{xx} = -2S_{ij}^{yy} \Rightarrow S_{ij}$$

where $\boldsymbol{S}_{ij}$ is a (3x3) matrix which is symmetric and of zero trace which characterizes the current state of relaxation for the nematic liquid crystal. Note that only one phase and orientational state is described by a particular ***S*** in which the system temperature is implicit.

Simulated Dynamics

Once there is a parametrized characterization of orientational order with a more generalized basis, the relaxation equation follows,

$$\tau_a \frac{\partial S_{\mu\upsilon}}{\partial t} - \xi_0^2 \Delta S_{\mu\upsilon} - \frac{1}{2\xi}\left(\varepsilon_{\parallel} - \varepsilon_{\perp}\right)\varepsilon_0 E_\mu E_\upsilon = 0$$

where the second term is the orientational order term, and the third term depends upon the external field.

The influence on the local orientation due to a neighboring volume with an order parameter of $S_{\chi\upsilon}$ is given by the cross product

$$\varepsilon_{\lambda\chi\nu} S_{\chi\nu}\left(\tau_a \frac{\partial S_{\mu\nu}}{dt} - \xi_0^2 S_{\mu\nu} - \frac{1}{2\xi}\left(\varepsilon_{\parallel} - \varepsilon_{\perp}\right)\varepsilon_0 E_\mu E_\nu\right) = 0$$

where ε is the Levi-Cevita antisymmetric isotropic tensor of rank 3. If $\boldsymbol{S}$ is uni-axial, as above with a nematic material, the previous equation reduces to

$$\varepsilon_{\lambda\chi\nu} n_\chi n_\nu\left(\gamma_1 \frac{\partial}{\partial t}\left(n_\nu n_\mu\right) - K\Delta\left(n_\nu n_\mu\right) - \xi_S \varepsilon_0 E_\mu E_\nu\right) = 0$$

where K is the traditional Frank elasticity constant that is measured experimentally from the material under simulation, and alpha is a normalization constant. Taking a finite-difference approximation to the last equation results in

$$n_\mu^{new} = \lambda\left\{(1 - 2d\alpha)n_\mu + \alpha\left[2d\left\langle n_\mu, n_\nu\right\rangle + \xi_S \varepsilon_0 E_\mu E_\nu\right]\right\}$$

where d is the finite-difference spatial discretization length.

So for a nematic, the result is not so surprising, where the integration time step multiplies terms that depend on the local spatial average of the director, the local field, and one additional normalized self-acting term.

Now, given an electric field $\boldsymbol{E}$, one can calculate the equilibrium director configuration, using the Laplace Solver.

The problem with the electric field calculation is that when ***n*** is anisotropic, it affects the local electric field, so the director configuration depends on the electric field, which depends on the director configuration, and so on. So the equilibrium director configuration must be calculated iteratively, with the electric field recalculated at every step. What would have been an algebraic solution to a linear Laplace's equation had to be modified to account for the local field perturbations (Fig 15).

In order to calculate the electric field, the following potential equation must be solved.

$$\left(\varepsilon_{\perp}+\Delta\varepsilon n_x^2\right)\frac{\partial^2}{\partial x^2}V+2\Delta\varepsilon n_x n_y\frac{\partial^2}{\partial x\partial y}V$$
$$+\Delta\varepsilon\left(2n_x\frac{\partial n_x}{dx}+n_x\frac{\partial n_y}{\partial y}+n_y\frac{\partial n_x}{\partial y}\right)\frac{\partial}{\partial x}V$$
$$+\Delta\varepsilon\left(2n_y\frac{\partial n_y}{dy}+n_y\frac{\partial n_x}{\partial x}+n_x\frac{\partial n_y}{\partial x}\right)\frac{\partial}{\partial y}V$$
$$+\left(\varepsilon_{\perp}+\Delta\varepsilon n_y^2\right)\frac{\partial^2}{\partial y^2}V=0$$

Then, of course, $\boldsymbol{E}$=-grad(V). So if $\Delta\varepsilon << \varepsilon_{\perp}$, the equation reduces to Laplace's equation, and the field is independent of the director configuration. (Note that while the potential function is linear in V it depends nonlinearly on the director field). Here the equation is written for two-dimensions for convenience, but the extension to an additional degree-of-freedom is straightforward. Again, the finite difference approximation was taken, and the system was iterated using a successive-over-relaxation scheme to speed convergence.

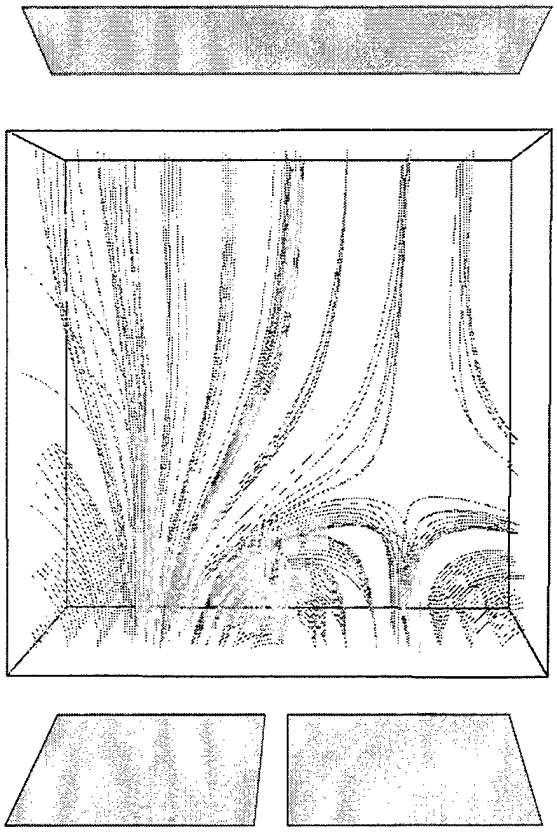

Figure 15 - A simulated equilibrium electric field configuration for a twelve-micron cell gap with two ten micron pixels, one at 3.5 volts and the other at 0 Volts across from a common grounded electrode at the top. The important feature of this simulation output is that the field is fairly homogenous across the top two thirds of the cell. This means that for the majority of the cell, the optical properties of the liquid crystal material which aligns with the field is identical over pixels with very different data. The electro-optic effects are only visibly different in the bottom third of the cell. This clearly indicates that a thinner cell-gap is appropriate.

Simulated Optics

Now, once we have arrived at an equilibrium director configuration, optical calculations can be performed. The optical simulation for the display modules began simply by following traditional implementations of the Jones calculus and were extended to approximations by Berreman[6] when inter-layer reflections became important in the smectic ferroelectric materials.

In short, there are several important characteristics in the performance of reflective LC cells: the contrast, the brightness (efficiency of light), the chromaticity, the switching speed, and the required switching voltage. These characteristics are determined by LC cell configuration, more specifically, the cell gap, twist angle, pretilt angle, polarizer direction, type of polarizer (circular, linear, or polarized beam splitter), and type of LC. It is a definite necessity to find the right LC configuration in order to achieve the required performance characteristics, which is what the liquid crystal behavior modeling tools are used for. There are commercial simulation packages currently available, however they are not only expensive, but also lack the flexibility we need and that we were able to build into our own software.

To summarize, the LC behavior modeling software is includes the following capabilities:

1) LC director calculation
2) Berremann's matrix calculation of light propagation inside LC
3) Different polarizers and light source options
4) Different LC cell type options (twisted nematic, homeotropic to twisted nematic, hybrid alignment, PI-cell,
5) Voltage-reflectance curve for all types of LC cell
6) Automatic optimization with genetic algorithm.

By simply inputting the required contrast, brightness and chromaticity parameters, our modeling tool can automatically find any matches in each of the known reflective LC modes; mixed-mode, self-compensated, reflective twisted nematic, and 63 degree twisted nematic cells. The modeling software also allows us to optimize LC cell configurations under very specific restrictions.

Not only does the modeling software allow for the capability to design LC cells to meet specified performance requirements, it also enables quick, cost-efficient research and development cycles, which in turn add to rapid overall prototyping cycles at reduced resource expenditure.

Optical Distortion Compensation Compiler

Once the liquid crystal cells and their interactions with driving electrodes and viewing and illumination optics are well understood, the actual design of the driving electronics is undertaken. This next design phase of the manufacturing process will use a combination of traditional commercial VLSI design tools with a state-of-the-art MicroDisplay product, The MicroDisplay Optical Distortion Compensation Compiler, to rapidly layout custom active matrix displays integrated with high performance control and interface logic in CMOS circuits. The MicroDisplay compiler has several unique capabilities. Foremost among these is the capability to compensate for smaller packages, cheaper lenses, and limited resolution in the very layout of the CMOS active-matrix pixel arrays.

There is a fundamental tradeoff between the complexity and weight of the optical system used to magnify and view the display versus the weight and inconvenience of large heavy optics. To assist in viewing MicroDisplays, a good microscope can provide a high quality narrow-field-of-view image, but is rather inconvenient to lug about. On the other hand, a simpler (shorter focal length), more lightweight optical system for wide-angle images introduces considerable distortion. Several companies have begun compensating for this distortion in artificially generated virtual reality displays by preprocessing the image data in real-time to pre-warp the image data before it is "distorted" by a small wide-angle optical system. Real-time image processing computers for non-local algorithms are still too large and are not portable. Truly portable systems require another solution.

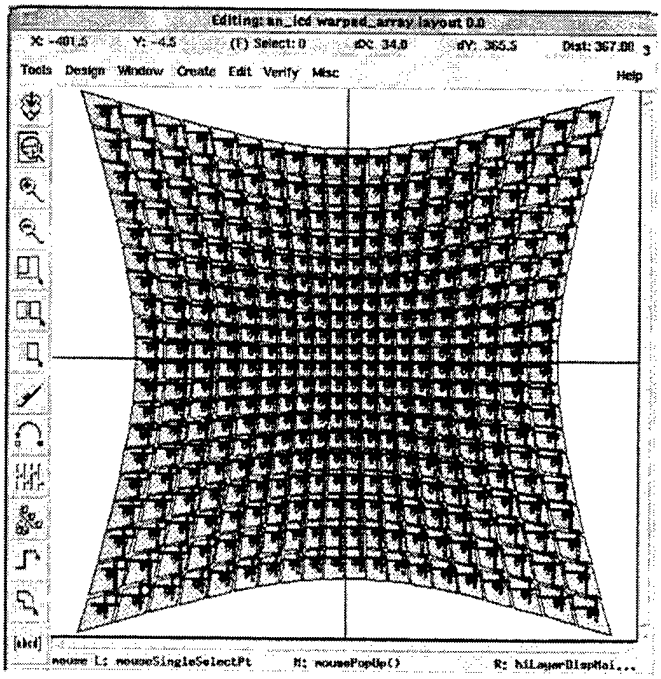

Figure 16 - A screen dump from the Microdisplay Compiler depicting the inverse distortion function for a LEEP-type optical system.

The solution developed at MIT was a tool that uses the automated layout of a VLSI pixel array in conjunction with an optical design CAD tool to compensate for optical distortions and aberrations (Fig 16). Ray tracing experiments through actual and simulated optics can generate a distortion function which is monotonically increasing with radius from the optical axis. Therefore, there exists an inverse function which can negate this nonlinear distortion. A third-order polynomial fit to the distortion function data provides a good approximation to the inverse function. This radially symmetric function is then used to position and scale the individual pixels of the display. Since the array is very regular, albeit of peculiar and specific form, a distortion compensation compiler was written to implement a scaleable architecture, where multi-sized chips can be "auto-instanced and routed" with the late-binding specification of only a few parameters such as DISTORTION_FUNCTION, CHROMATIC_ABBERATION, ARRAY_WIDTH, PACKING_DENSITY, and so forth. Figure 16 shows the layout of a small prototype device intended to compensate for a typical short-focal-length magnifier distortion. The current MicroDisplay compiler even compensates for varying warped pixel capacitances by adjusting the size of the buried storage capacitor for each pixel. The MicroDisplay compiler was written in C++, reads lens characterization output from the CODE V optical design CAD tool, and outputs complete pixel arrays in both the CADENCE VLSI design tool language called SKILL and also in CIF. This silicon compiler technology alone allows very rapid display customization and prototyping. With the added techniques for compensating for optical system distortion and aliasing (Fig 17), virtual imaging device packages can be made much smaller.

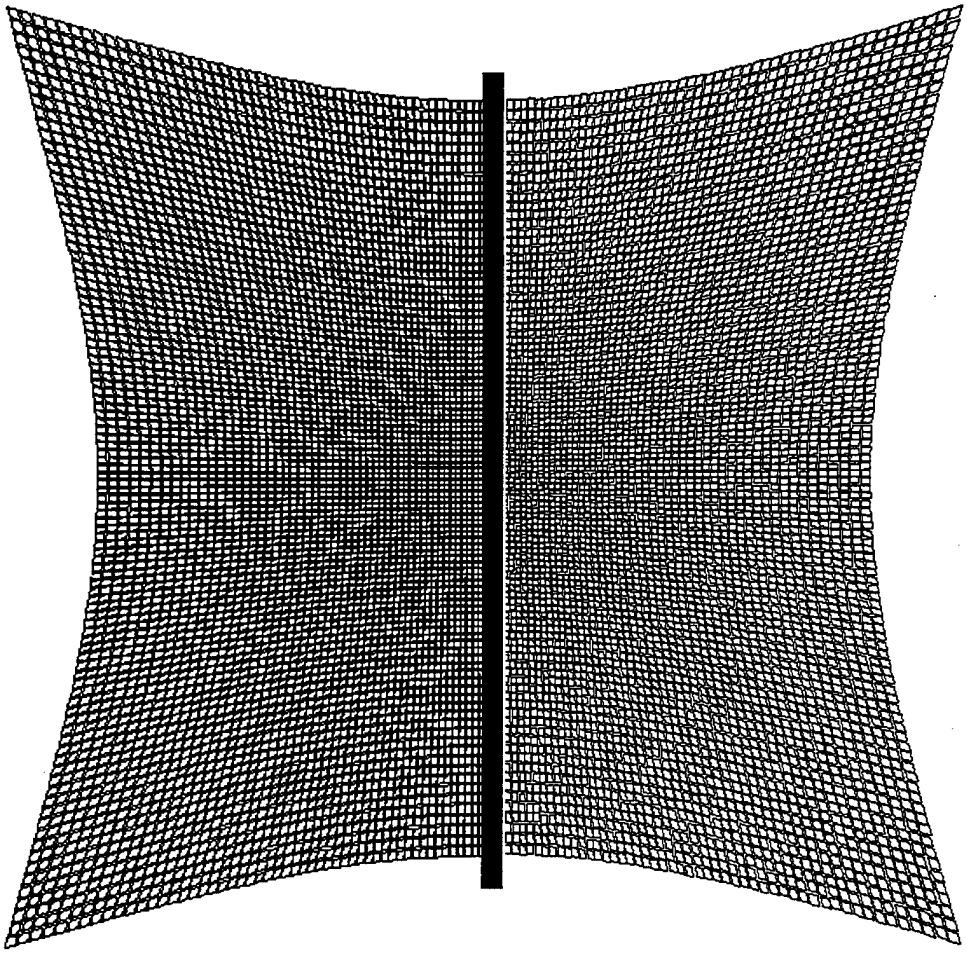

Figure 17 - The Microdisplay compiler output for the LEEP-type optical pre-distortion function with the right half of the pixel array "jittered" to reduce aliasing.

Resulting technology

The most efficient video-rate liquid crystal material technology in the industry

- Fast-switching LC operating modes to achieve 8-bit color resolution in 180 Hz field sequential color mode
- Wide viewing angle LC operating modes suitable for use in direct-view wristwatch-type video displays
- Highly reflective pixel mirror designs for the most optically efficient microdisplays in the industry
- High-performance microdisplay eyepiece designs

In the field of liquid crystal materials, MicroDisplay has developed the lowest-power operating mode that is fast enough and has sufficient contrast to show full-motion video in full color. This groundbreaking LC mode has the lowest switching voltage threshold in the industry with the fastest reported switching speeds. The new mode also has a very wide viewing-angle that permits use in direct view without any imaging optics. This industry-leading optical performance has been achieved using standard nematic liquid crystal material. The use of these commonly available materials and preparation methods means that MicroDisplay's new proprietary operating mode can be manufactured at low cost with easily available materials and processing equipment.

Resulting applications

Another set of materials and process innovations has been completed in cooperation with our CMOS foundry partners. MicroDisplay has cooperated with Chartered Semiconductor to develop and optimize their CMOS process to fabricate the highest-performance pixel mirrors in the industry. With a 92% reflection off of the pixel electrodes, MicroDisplay has achieved unmatched optical efficiency.

Illumination and magnification of a microdisplay is a specialty that is only fully understood by a few industry engineers. One look through the Company's LookingGlass™ eyepiece designed for the color VGA microdisplay clearly demonstrates the expertise of MicroDisplay's optics engineers. The 3-inch eye-relief combined with uniform illumination over a wide eye-box is unique in the industry. The entire viewing system including the lenses and housing can be fabricated from low-cost plastic materials.

5 CONCLUSIONS

Technology Conclusions

We have demonstrated the feasibility of cost-effective integrated circuitry for portable display systems by showing that additional decoding circuitry does not have a significant detrimental impact on device area requirements or production yield. We have demonstrated the validity of the product, producibility, and cost reduction cycle based on higher levels of integration for each generation. All of these conclusions are fundamentally supported by a series of successful prototype demonstration devices and deliverables that are now ready for productization.

Recommendations

The technology has been demonstrated along with the ASIC style approach of developing complete display-systems on a chip. The design tools and development infrastructure are in place, and have been validated with these successful designs.

The technology described above has now successfully transitioned into several follow-on programs to develop next-generation consumer and military products. The commercialization effort continues.

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